AMENDMENTS TO THE CLAIMS

Please cancel claims 1-10, and add new claims 11-24, as shown in the following list of claims:

Claims 1-10. (Canceled)

Claim 11. (New). A method of manufacturing a semiconductor device having first and second semiconductor chips, comprising:

preparing the first and second semiconductor chips, the first semiconductor chip having a semiconductor substrate area which is free of the formation of transistors which generate heat when in operation, and a transistor forming area; and

mounting the second semiconductor chip on the first semiconductor chip so as to arrange the second semiconductor chip just above the substrate area of the first semiconductor chip.

Claim 12. (New) The method according to claim 11, wherein the semiconductor substrate area is surrounded by the transistor forming area.

Claim 13. (New) The method according to claim 11, wherein the semiconductor substrate area is an approximately central area of the first semiconductor chip.

Claim 14. (New) The method of claim 11, wherein the semiconductor substrate area is larger than the area of the second semiconductor chip.

Claim 15. (New) The method of claim 11, wherein:

the first semiconductor chip has at least one first electrode formed on the periphery of the semiconductor substrate area, at least one second electrode formed on the periphery of the transistor forming area, and a plurality of leads disposed around said first semiconductor chip;

the second semiconductor chip has at least one third electrode formed thereon; and

the method further comprises:

connecting the first electrode of said first semiconductor chip and the third electrode of said second semiconductor chip with at least one first metal wire; and

connecting said second electrode of said first semiconductor chip and said leads with at least one second metal wire.

Claim 16. (New) The method according to claim 15, wherein said third electrode of said second semiconductor chip is electrically connected to said second electrode of said first semiconductor chip through a transistor formed within the transistor forming area of said first semiconductor chip.

Claims 17. (New) The method according to claim 11, further comprising:

sealing said first and second semiconductor chips, said first and second metal wires and some of said leads with an encapsulating resin.

Claim 18. (New). A method of manufacturing a semiconductor device having first and second semiconductor chips, comprising:

preparing the first and second semiconductor chips, the first semiconductor chip having a first area which is free of the formation of elements which generate heat when in operation, and a second area which surrounds the first area; and

mounting the second semiconductor chip on the first semiconductor chip so as to arrange the second semiconductor chip just above the first area of the first semiconductor chip.

Claim 19. (New) The method according to claim 18, wherein a microcontroller used as a mask ROM is formed on the first area, and said second semiconductor chip serves a function of a flash memory.

Claim 20. (New) The method according to claim 18, wherein the semiconductor substrate area is an approximately central area of the first semiconductor chip.

Claim 21. (New) The method of claim 18, wherein the semiconductor substrate area is larger than the area of the second semiconductor chip.

Claim 22. (New) The method of claim 18, wherein:

the first semiconductor chip has at least one first electrode formed on the periphery of the first area, at least one second electrode formed on the periphery of the second area, and a plurality of leads disposed around said first semiconductor chip;

the second semiconductor chip has at least one third electrode formed thereon; and

the method further comprises:

connecting the first electrode of said first semiconductor chip and the third electrode of said second semiconductor chip with at least one first metal wire; and

connecting said second electrode of said first semiconductor chip and said leads with at least one second metal wire.

Claim 23. (New) The method according to claim 22, wherein said third electrode of said second semiconductor chip is electrically connected to said second electrode of said first semiconductor chip through a transistor formed within the second area of said first semiconductor chip.

Claims 24. (New) The method according to claim 18, further comprising:

sealing said first and second semiconductor chips, said first and second metal wires and some of said leads with an encapsulating resin.